ABSTRACT

Each processor in a distributed shared memory system has an associated memory and a coherence directory. The processor that controls a memory is the Home processor. Under certain conditions, another processor may obtain exclusive control of a data block by issuing a Load Lock instruction, and obtaining a writeable copy of the data block that is stored in the cache of the Owner processor. If the Owner processor does not complete operations on the writeable copy of the data prior to the time that the data block is displaced from the cache, it issues a Victim To Shared message, thereby indicating to the Home processor that it should remain a sharer of the data block. In the event that another processor seeks exclusive rights to the same data block, the Home processor issues an Invalidate message to the Owner processor. When the Owner processor is ready to resume operation on the data block, the Owner processor again obtains exclusive control of the data block by issuing a Read-with Modify Intent Store Conditional instruction to the Home processor. If the Owner processor is still a sharer, a writeable copy of the data block is sent to the Owner processor, who completes modification of the data block and returns it to the Home processor with a Store Conditional instruction.